In the Claims:

Please amend claims 1, 6, 8, and 12. The claims are as follows:

1. (Currently amended) A method for chip separation, the method comprising the steps of:

(a) providing a semiconductor substrate;

(b) forming first and second device regions in and at top of the semiconductor substrate,

wherein the first and second device regions are separated by a semiconductor border region of the semiconductor substrate;

(c) forming N interconnect layers, in turn, directly above the semiconductor border region and the first and second device regions,

wherein N is a positive integer greater than one,

wherein each layer of the N interconnect layers comprises an etchable portion directly above the semiconductor border region,

wherein the etchable portions of the N interconnect layers form a continuous etchable block directly above the semiconductor border region, and

wherein the entire continuous etchable block comprises essentially a same material throughout the entire continuous etchable block;

(d) removing the continuous etchable block by etching; and

(e) cutting with a laser through the semiconductor border region via an empty space of the removed continuous etchable block.

2. (Original) The method of claim 1, wherein the continuous etchable block comprises a material which is etchable by wet etching.

3. (Original) The method of claim 1, wherein the continuous etchable block comprises copper.

4. (Original) The method of claim 1, wherein the step of removing the continuous etchable block is performed by wet etching.

5. (Original) The method of claim 1, further comprising the steps of:

back-side grinding a back surface of the semiconductor substrate; and then

applying a dicing tape to the back surface of the semiconductor substrate before the step of removing the continuous etchable block by etching.

6. (Currently amended) ~~The method of claim 1,~~ A method for chip separation, the method comprising the steps of:

(a) providing a semiconductor substrate;

(b) forming first and second device regions in and at top of the semiconductor substrate,

wherein the first and second device regions are separated by a semiconductor border

region of the semiconductor substrate;

(c) forming N interconnect layers, in turn, directly above the semiconductor border region and the first and second device regions,

wherein N is a positive integer greater than one,

wherein each layer of the N interconnect layers comprises an etchable portion directly above the semiconductor border region,

wherein the etchable portions of the N interconnect layers form a continuous etchable block directly above the semiconductor border region, and

wherein the entire continuous etchable block comprises essentially a same material;

(d) removing the continuous etchable block by etching; and

(e) cutting with a laser through the semiconductor border region via an empty space of the removed continuous etchable block,

wherein the semiconductor substrate comprises bulk silicon, and

wherein, after the step of removing the continuous etchable block by etching, but before the step of cutting by the laser through the semiconductor border region, the method further comprises the step of wet etching a portion of the semiconductor border region so as to form a V-shaped trench in the semiconductor border region.

7. (Original) The method of claim 1, wherein the step of removing the continuous etchable block

by etching is performed until a surface of the semiconductor border region is exposed to the atmosphere.

8. (Currently amended) ~~The method of claim 1,~~ A method for chip separation, the method comprising the steps of:

(a) providing a semiconductor substrate;

(b) forming first and second device regions in and at top of the semiconductor substrate,

wherein the first and second device regions are separated by a semiconductor border region of the semiconductor substrate;

(c) forming N interconnect layers, in turn, directly above the semiconductor border region and the first and second device regions,

wherein N is a positive integer greater than one,

wherein each layer of the N interconnect layers comprises an etchable portion directly above the semiconductor border region,

wherein the etchable portions of the N interconnect layers form a continuous etchable block directly above the semiconductor border region, and

wherein the entire continuous etchable block comprises essentially a same material;

(d) removing the continuous etchable block by etching; and

(c) cutting with a laser through the semiconductor border region via an empty space of the removed continuous etchable block,

wherein each layer of the N interconnect layers further comprises first and second chip edge portions and first and second isolation portions directly above the semiconductor border region, and

wherein the first chip edge portions of the N interconnect layers form a first continuous chip edge block directly above the semiconductor border region,

wherein the second chip edge portions of the N interconnect layers form a second continuous chip edge block directly above the semiconductor border region,

wherein the first isolation portions of the N interconnect layers form a first continuous isolation block directly above the semiconductor border region,

wherein the second isolation portions of the N interconnect layers form a second continuous isolation block directly above the semiconductor border region,

wherein the continuous etchable block is sandwiched between the first and second continuous isolation blocks,

wherein the first continuous isolation block is sandwiched between the continuous etchable block and the first continuous chip edge block,

wherein the second continuous isolation block is sandwiched between the continuous etchable block and the second continuous chip edge block, and

wherein the first and second isolation portions comprise a material which is essentially not affected by the step of removing the continuous etchable block by etching.

9. (Original) The method of claim 8, wherein the first and second continuous chip edge blocks comprise a same material as the continuous etchable block.

10. (Original) The method of claim 9, wherein the same material of the first and second continuous chip edge blocks and the continuous etchable block comprises copper.

11. (Original) The method of claim 8, wherein the first and second continuous chip edge blocks comprise a material that is essentially not affected by the laser.

12. (Currently amended) A method for chip separation, the method comprising the steps of:

(a) providing a semiconductor substrate;

(b) forming first and second device regions and a filled deep trench in and at top of the semiconductor substrate,

wherein the first and second device regions are separated by a semiconductor border region of the semiconductor substrate, and

wherein the semiconductor border region comprises the filled deep trench;

(c) forming N interconnect layers, in turn, directly above the border region and the first and second device regions,

wherein N is a positive integer greater than one,

wherein each layer of the N interconnect layers comprises an etchable portion directly above the filled deep trench,

wherein the etchable portions of the N interconnect layers form a continuous etchable

block directly above the filled deep trench, and

wherein the entire continuous etchable block comprises essentially a same material throughout the entire continuous etchable block;

(d) removing the continuous etchable block by etching; and

(e) cutting with a laser through the filled deep trench via an empty space of the removed continuous etchable block.

13. (Original) The method of claim 12, wherein the filled deep trench comprises a material which can be easily cut through by the laser.

14. (Original) The method of claim 12, wherein the filled deep trench comprises a material selected from the group consisting of polysilicon and silicon oxide.

15. (Withdrawn) A semiconductor structure, comprising:

(a) first and second device regions in and at top of a semiconductor substrate, wherein the first and second device regions are separated by a semiconductor border region of the semiconductor substrate; and

(b) N interconnect layers directly above the border region and the first and second device regions,

wherein N is a positive integer,

wherein each layer of the N interconnect layers comprises an etchable portion directly above the semiconductor border region, and

wherein the etchable portions of the N interconnect layers form a continuous etchable

block directly above the semiconductor border region.

16. (Withdrawn) The structure of claim 15, wherein the continuous etchable block comprises a material which is etchable by wet etching.

17. (Withdrawn) The structure of claim 15, wherein the continuous etchable block comprises copper.

18. (Withdrawn) The structure of claim 15,

wherein each layer of the N interconnect layers further comprises first and second chip edge portions and first and second isolation portions directly above the semiconductor border region, and

wherein the first chip edge portions of the N interconnect layers form a first continuous chip edge block directly above the semiconductor border region,

wherein the second chip edge portions of the N interconnect layers form a second continuous chip edge block directly above the semiconductor border region,

wherein the first isolation portions of the N interconnect layers form a first continuous isolation block directly above the semiconductor border region,

wherein the second isolation portions of the N interconnect layers form a second continuous isolation block directly above the semiconductor border region,

wherein the continuous etchable block is sandwiched between the first and second continuous isolation blocks,

wherein the first continuous isolation block is sandwiched between the continuous etchable block and the first continuous chip edge block, and

wherein the second continuous isolation block is sandwiched between the continuous etchable block and the second continuous chip edge block.

19. (Withdrawn) The structure of claim 18, wherein the first and second continuous chip edge blocks comprise a same material as the continuous etchable block.

20. (Withdrawn) The method of claim 19, wherein the same material of the first and second continuous chip edge blocks and the continuous etchable block comprises copper.